

ABSTRACT OF THE INVENTION

A composite layer of low k silicon oxide dielectric material is formed on an oxide layer of an integrated circuit structure on a semiconductor substrate having closely spaced apart metal lines thereon. The composite layer of low k silicon oxide dielectric material exhibits void-free  
5 deposition properties in high aspect ratio regions between the closely spaced apart metal lines, deposition rates in other regions comparable to standard k silicon oxide, and reduced via poisoning characteristics. The composite layer of low k silicon oxide dielectric material is formed by depositing, in high aspect ratio regions between closely spaced apart metal lines, a first layer of low k silicon oxide dielectric material exhibiting void-free deposition properties until the resulting deposition of low k silicon oxide dielectric material reaches the level of the top of the metal lines on the oxide layer. A second layer of low k silicon oxide dielectric material, having a faster deposition rate than the first layer, is then deposited over the first layer up to the desired overall thickness of the low k silicon oxide dielectric layer. In a preferred embodiment, the steps to form the resulting composite layer of low k silicon oxide dielectric material are all carried out in a single vacuum processing apparatus without removal  
10 of the substrate from the vacuum apparatus.  
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